IN THE CLAIMS:

1. (Once amended) A semiconductor chip package, comprising:

a substrate having a plurality of terminals;

a semiconductor chip on said substrate, said semiconductor chip including,

a plurality of [inner] bond pads,

a first insulation layer covering said chip,

a first plurality of holes in said first insulation layer exposing said [inner] bond pads,

a metal layer [disposed] deposited over said first insulation layer [in] to form an electrical contact with said [inner] bond pads,

a second insulation layer [disposed] deposited over said metal layer, and

a second plurality of holes in said second insulation layer exposing selected portions of said metal layer to form external connection points such that said metal layer routes respective bond pads to corresponding external connection points; and

electrically conductive epoxy [disposed] applied between said external connection points of said semiconductor chip and said terminals of said substrate, thereby electrically connecting said semiconductor chip to said substrate.

4. (Once amended) A semiconductor chip package as in Claim 1, wherein said semiconductor chip is [disposed] placed on said substrate face-down such that said external connection points are positioned directly above said terminals on said substrate.

5. (Once amended) A semiconductor chip package as in Claim 1, wherein said semiconductor chip is [disposed] placed on said substrate face-up such that said external connection points face-away from said terminals on said substrate.

11. (Once amended) A method for producing a multichip package, said method comprising the steps of:

providing [inner] bond pads on said chip;

covering said chip with a first insulation layer;

forming a first plurality of holes in said first insulation layer to expose said [inner] bond pads;

[disposing] depositing a metal layer over said first insulation layer such that said metal layer is in electrical contact with said [inner] bond pads;

[disposing] depositing a second insulation layer over said metal layer;

exposing selected portions of said metal layer to form external connection points such that said metal layer routes respective bond pads to corresponding external connection points;

providing a substrate having a plurality of terminals; and

[disposing] applying conductive epoxy between said external connection points of said chip and said terminals of said substrate to electrically connect said chip to said substrate.

12 11
9 (Once amended). A method as in Claim 8, further comprising the step of [disposing] placing said chip ~~is~~ on said substrate face-down such that said external connection points are positioned directly above said terminals on said substrate.

---

14 11
11. (Once amended) A method as in Claim 8, further comprising the step of [disposing] placing said chip [substrate] face-up on said substrate such that said external connection points face-away from said terminals on said substrate.

17
14. (Once amended) A flip-chip package, comprising:

a printed circuit board having a plurality of terminals;

a flip-chip including,

four edges;

a plurality of [inner] bond pads,

a first insulation layer covering said flip-chip,

a first plurality of holes in said first insulation layer exposing said [inner] bond pads,

a metal layer [disposed] deposited over said first insulation layer in electrical contact with said [inner] bond pads

a second insulation layer [disposed] deposited over said metal layer, and

a second plurality of holes in said second insulation layer exposing selected portions of said metal layer to form external connection points such that said metal layer routes respective bond pads to corresponding external connection points, said external connection points being located on said flip-chip internally from said edges;

said flip-chip [disposed] placed on said printed circuit board face-down such that said external connection points are positioned directly above said terminals on said printed circuit board; and

electrically conductive epoxy [disposed] applied between said external connection points of said flip-chip and said terminals of said printed circuit board, thereby electrically connecting said chip to said printed circuit board.

18
15. (Once amended) A chip package, comprising:

a printed circuit board having a plurality of terminals;

a chip including,

four edges;

a plurality of [inner] bond pads,

a first insulation layer covering said chip,

a first plurality of holes in said first insulation layer exposing said [inner] bond pads,

a metal layer [disposed] deposited over said first insulation layer in electrical contact with said [inner] bond pads

a second insulation layer [disposed] deposited over said metal layer,

a second plurality of holes in said second insulation layer exposing selected portions of said metal layer to form external connection points such that said metal layer routes respective bond pads to corresponding external connection points, said external connection points being located along said edges of said chip, and

beveled edge walls located at the outer edges of said chip and sloping toward the center of said chip;

said chip [disposed] placed on said printed circuit board face-up; and electrically conductive epoxy [disposed] applied along said beveled edge walls between said external contact points of said chip and said terminals of said printed circuit board, thereby electrically connecting said chip to said printed circuit board.

Add Claims 16-18, as follows:

8
16. The package as in Claim 1 including means for maintaining a minimum bond thickness between said chip and said substrate.

9 10
17. The package as in Claim 16 wherein said means for maintaining include at least one sphere of known thickness which lies between said external connection points and said terminals.

10 9
18. The package as in Claim 17 wherein said at least one sphere is a glass sphere.

28